that solder bump interconnections 16 do not reflow when attaching microelectronic package to the substrate.

(15) In an alternate embodiment, as depicted in FIG. 5, a similar process as the preferred embodiment is used to cover an integrated circuit die 112 with a polymeric precursor. A polymeric encapsulant 138, however, covers integrated circuit die 112 but does not underfill die 112. In this case, the viscosity and surface tension of the polymeric precursor and the gap 122 are such that underfilling of die 112 does not occur. Die 112 may substantially collapse toward carrier substrate 164 such that gap 122 is approximately 25 microns. Preventing underfill of die 112 is preferable when access to the active face 120 of die 112 is necessary, as in the case of providing heat dissipation by applying a thermally conductive material between the active face 120 of die 112 and carrier substrate 164. Preventing underfill of die 112 may be accomplished if the filler particles are large, if gas is entrapped in gap 122, if cavity walls or solder columns provide drag on the precursor, or for fine pitch interconnects. Without underfill, compliance issues between die 112 and carrier substrate 164 are minimized. Lack of underfill will also result for fine pitch solutions, typically less than about 6 mils (150 microns), that will prevent uniform flow of the mold material past substrate bond pads 142 and under die 112. This leads to an assembly that is more robust to the presence of moisture, and the possibility of delamination-induced failure is eliminated.

(16) In a further alternate embodiment, as depicted in FIG. 6, a polymeric encapsulant 238 extends partially under integrated circuit die 212. A similar process is used as in the preferred embodiment. However, the integrated circuit die 212 includes a plurality of solder bump interconnections 216 that are formed about the perimeter of die 212. A polymeric encapsulant 238 partially underfills a portion of gap 222 about solder bump interconnections 216 formed about the perimeter of die 212 but does not underfill the center portion of die 212. This is accomplished if steps are not taken to intentionally remove the air from gap 222 during underfilling. Solder bump interconnections 216 may be underfilled to ensure reliability, but additional process engineering to remove the air void is not required, thereby leading to a simplified manufacturing process.

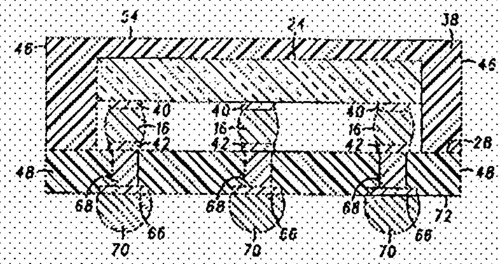

FIG.5

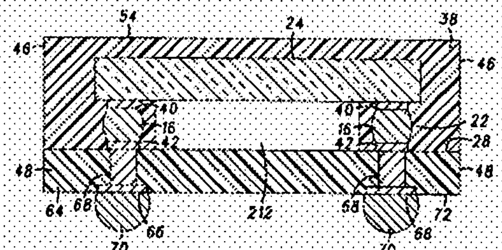

FIG.6

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mentioned above can be slightly modified to suit these applications. For pressure controlled sensor packaging, a cavity 21 will be created in the substrate 2, as opposed to an access hole 3 that was mentioned above. The sensing element 4 (e.g. accelerometer) will then be bonded using the flip chip method. Underfill material 14 is then applied from the backside of the sensor chip (front side of the substrate), in an environment where the gas and pressure are controlled. Due to capillary forces the underfill material would fill the entire common gap between the substrate 2 and the sensor chip 1 without covering the sensing element 4. This also provides a very effective method for sealing off the sensing element 4 from the outside environment and providing a controlled pressure/controlled gas environment inside the cavity 26. FIG. 6 shows a schematic of this approach. As mentioned previously, additional encapsulant can be applied around the underfill material 14 and protective layers can be deposited on either side of the package. The aforementioned approach can also be applied for monolithic sensors and hybrid packaging of electronics components along with sensors. For example in a monolithic sensor, the electronic components can be located on the sensor chip in the area above the cavity.

(15) An alternative method for sensor packaging utilizes a cap 22 and a technique similar to the aforementioned flip chip bonding method to provide a controlled pressure environment for the sensing element to operate in. This cap 22 can be made from various materials such as silicon, glass, ceramics, etc. Using dummy bumps 23, the cap 22 can be flip chip bonded to pads on the substrate 2. The underfill method 14 is then followed as previously mentioned. This method of applying the underfill material allows the area under the cap to be sealed off, thus providing a controlled pressure environment for the sensing element to operate in. The conductive pads 24 on the sensor chip 1 would be wire bonded 12 to pads 25 on the substrate 2. Metal lines 8, would then transfer the electric signals from these pads 25 to pads 6 located on the

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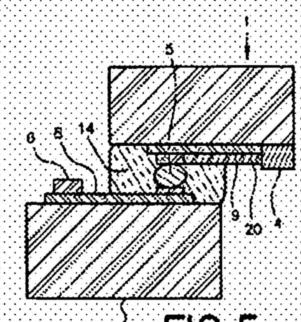

FIG.5

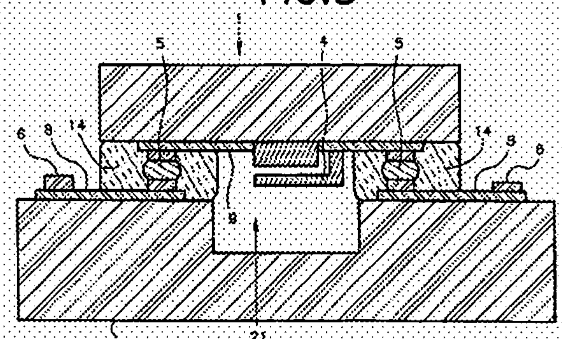

FIG.6

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around the ball electrodes 4a, 4b, . . . , 4g, . . . in FIG. 22, they may enclose all four surfaces to form a closed concave box region. In the plan view of FIG. 22, the patterns of the top surfaces of the substrate-cite interconnects 3a, 3b, . . . , 3g, . . . , exposed in the surrounding gap around the semiconductor chip 1, can be slightly recognized. And the top surfaces of the substrate-cite interconnects 3a, 3b, . . . ,3g, . . . , each exposed on the ball electrode mounting regions, with gaps in the periphery of the bumps 6a, . . . , 6g, can be recognized. Other portions of the substrate-cite interconnects 3a, 3b, . . . , 3g, . . . are hidden under the dielectric spacers 21.

[0099] FIG. 23 is a cross sectional view taken on line XXIII-XXIII in FIG. 22, showing that the semiconductor chip 1 is mounted on the first main surface of the module substrate 2 by the flip chip configuration, facing the top surface downward, on which the patterns of the integrated circuits are delineated. The dielectric spacer 21 has the same thickness as the semiconductor chip 1, more accurately the thickness essentially equal to the "effective thickness of the semiconductor chip 1" including the bump height. More definitely, the thickness of the dielectric spacer 21 may be determined taking into account the bump height and the thickness of the first heat conductive material 9.

[0100] As shown in the plan view of FIG. 22, the dielectric spacers 21 encloses around the three sides of the ball electrodes 4a and 4g. However, in the cross sectional view shown in FIG. 23, only one side of the dielectric spacer 21 located on the cross section can be seen. That is, the dielectric spacer 21 constitutes a concave box opened towards the edge portion (peripheral region) of the module substrate 2 at the each position of the ball electrodes 4a, . . . , 4g, ... Other structure and materials are essentially similar to those already explained in the first embodiment with FIGS. 2 to 4, and the overlapped description or the redundant description is omitted in the sixth embodiment.

[0101] When the same material as the module substrate 2 ...

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FIG.22

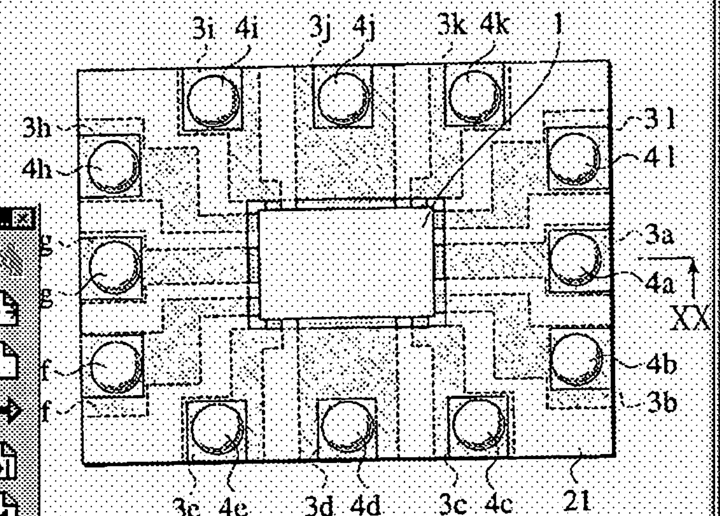
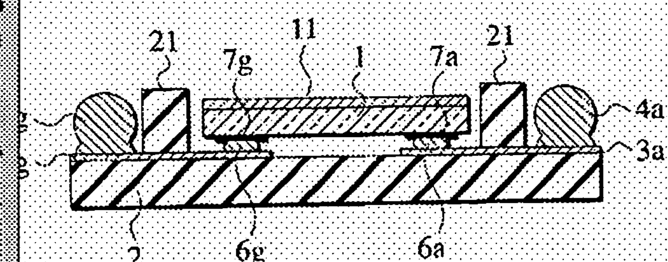


FIG.23



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